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Conformal Smart LEC - Cadence Design Systems

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Conformal ECOs at Marvell during pre-mask stage. We have done multiple ECOs using Conformal automated flow on various projects for the past few years. Below is the data for •Example 1 - Block A - Pre-mask ECO was done inside a control block which was instanced multiple(12) times. ECO fix involved combinational logic change in control block.

Practical ECOs using Conformal ECO tool - Cadence

Cadence ® Conformal ® Equivalence Checker (EC) makes it possible to verify and debug multi-million-gate designs without using test vectors. It offers the industry's only complete equivalence checking solution for verifying SoC designs—from RTL to final LVS netlist

(SPICE)—as well as FPGA designs.

Conformal Equivalence Checker - Cadence Design Systems

Cadence Conformal suite of tools contains a tool called Logic Equivalence Checker or LEC. Section 4 of this tutorial describes how to formally verify that the synthesized design is functionally equivalent to the RTL description using LEC. This section can be skipped if one chooses to use Formality for equivalence checking.

Digital Logic Synthesis and Equivalence Checking Tools ...

LEC comprises of three steps as shown below: Setup Mode, Mapping Mode and Compare Mode. Fig-1. Logical Equivalence Check flow diagram. There are various EDA tools for performing LEC, such as Synopsys Formality and Cadence Conformal. We are considering Conformal tool as a reference for the purpose of explaining the importance of LEC.